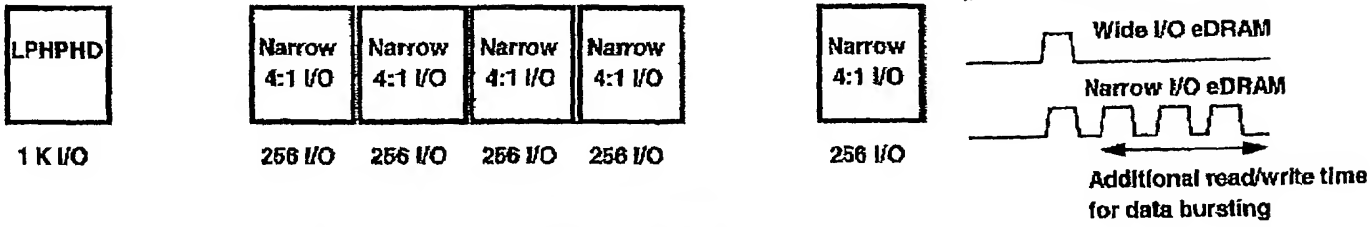
Single Cycle Read/Write/WriteBack Pipeline, Full-Wordline I/O DRAM Architecture with Enhanced Write and Single Ended Sensing

APPENDIX

Thirteen figures are attached as appendix pages A2 to A14, shematically showing examples of embodiments of the invention.

eDRAM Macro Comparison



Narrow I/O penalty: either 4 x macro power and area or slower performance

LP, HP => Wide I/O architecture => Single ended, small swing sensing (x-couple SA => more power !!)

Power saving and performance improvement by full word-line wid I/O and small swing sensing

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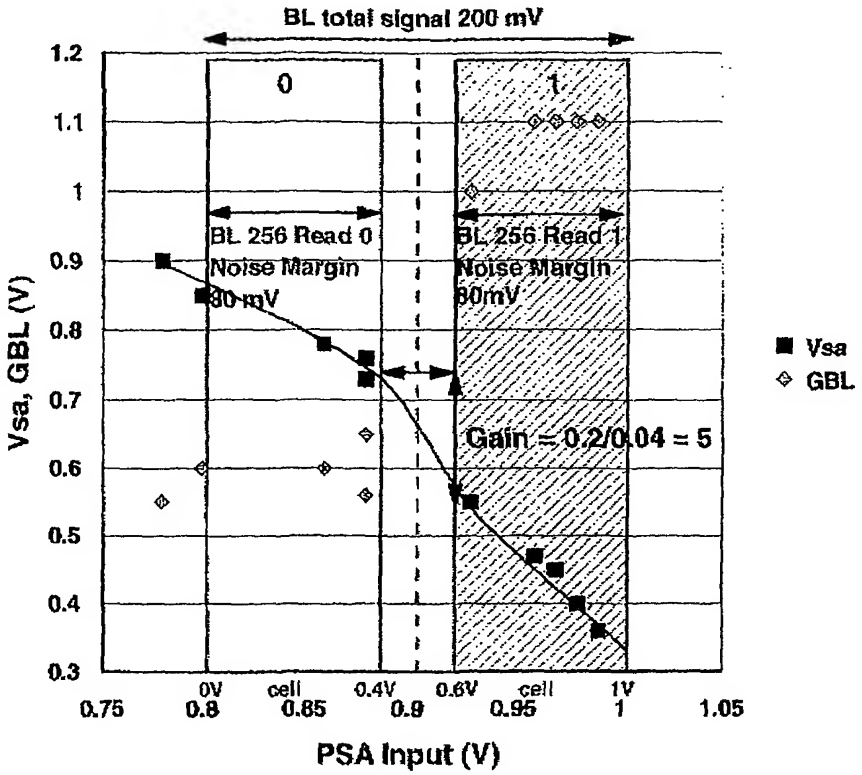
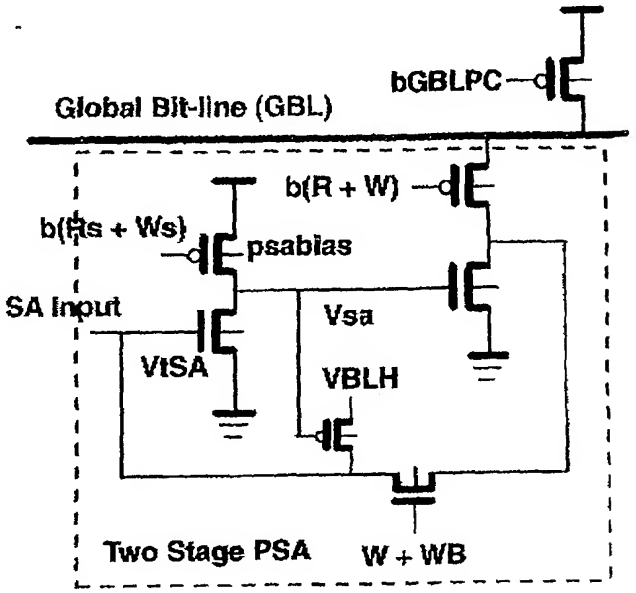
Sense Amplifier Characteristic and Margin



VBLH = 1 V, VDD = 1.1 V, VLL = 0.5 V
Cell transfer ratio: BL 128 = 1/3, BL 256 = 1/5

	Cell	BL 128	BL 256
0	Best case 0 V	0.67 V	0.8 V
0	Worst case 0.4 V	0.8 V	0.88 V
1	Worst case 0.6 V	0.87 V	0.92 V
1	Best case 1 V	1.0 V	1.0 V

	PSA Gain
Stage1	0.20 / 0.04 = 5
Stage1 (av)	0.52 / 0.20 = 2.6
Two stage	0.40 / 0.04 = 10
Two stage (av)	0.50 / 0.20 = 2.5



VBLH = 1 V, VDD = 1.1 V, VLL = 0.5 V
Cell transfer ratio: BL 128 = 1/3, BL 256 = 1/5

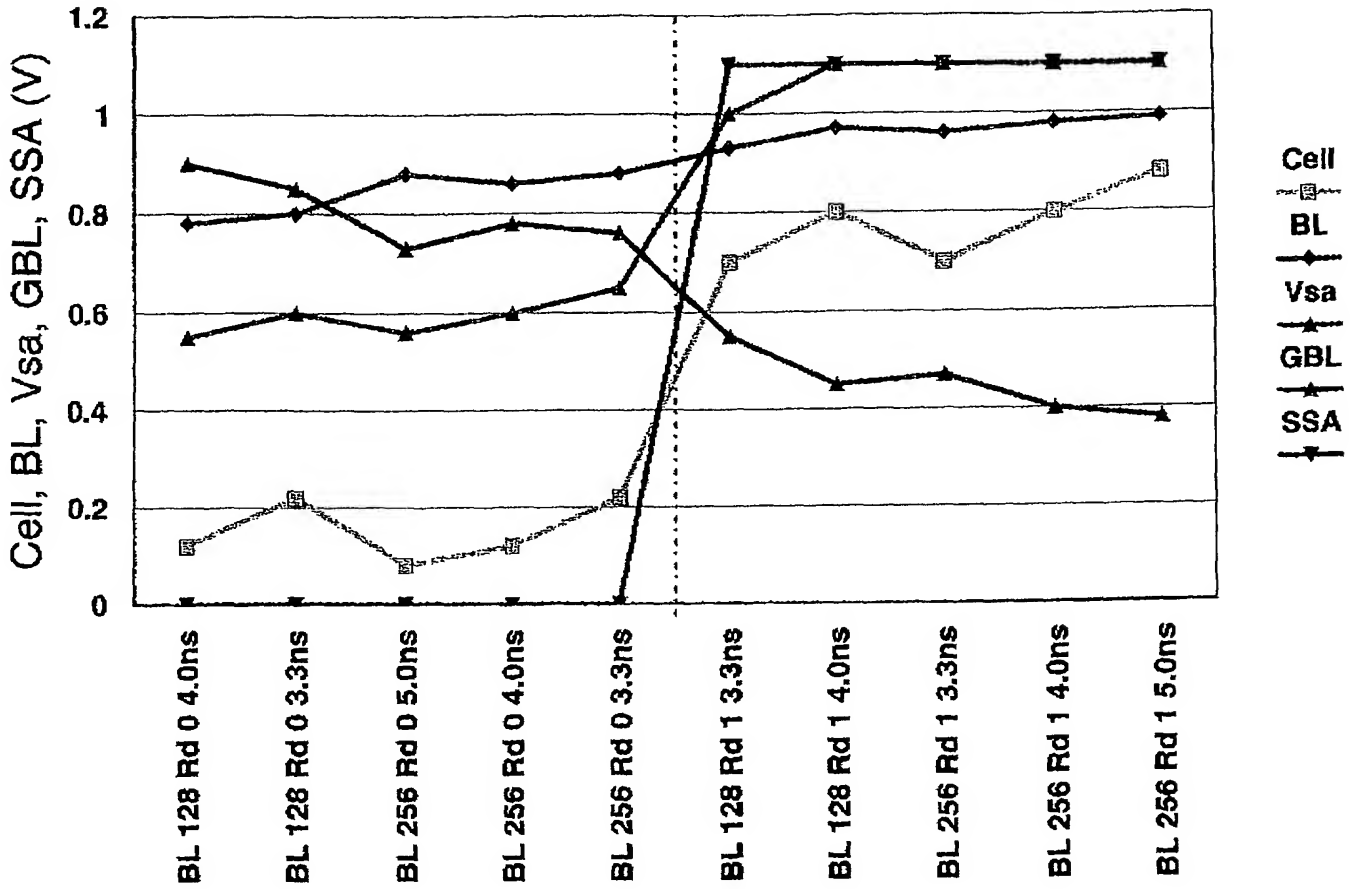
	VBL	Vsa	VGBL
Read 0 (wc):	0.75V(BL 128)	0.95 V	0.5 V
	0.88V(BL 256)	0.75 V	0.5 V
Read 1:	1 V	0.35 V	1 V
Write 0:	0 V	1 V	0.5 V
Write 1:	1 V	0.2 V	1 V

VBL(read1) > VrefSA + VtSA >= VBL(read0)
SAVref = 0.2 V, SAVt = 0.6 V (HVt nfet) or
SAVref = 0 V, psabias = - 0.5 V st VtSA ~ 0.8 V

1st Stage	W pfet/nfet	700 nm / 400 nm
	Vt pfet/nfet	0.7 V / 0.8 V
2nd Stage	W pfet/nfet	8 u / 3 u
	Vt pfet/nfet	0.3 V / 0.3 V

A3

Cell, BL, Vsa, GBL, SSA Voltages



VBLH = 1 V, VDD = 1.1 V, VLL = 0.5 V
Cell transfer ratio: BL 128 = 1/3, BL 256 = 1/5

A4

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Short Cycle R/W/r Pipeline with Concurrent Operations

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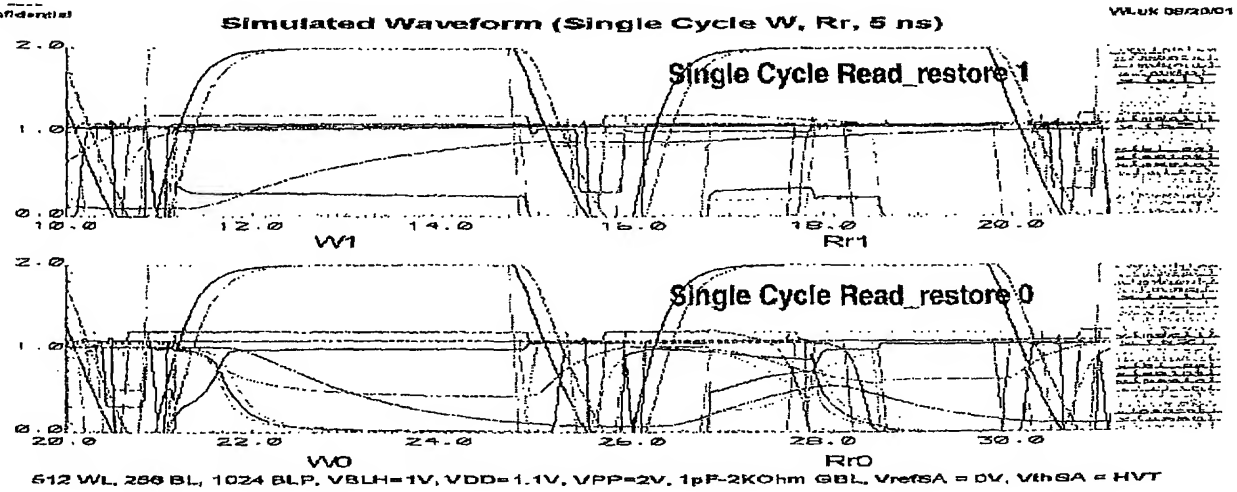

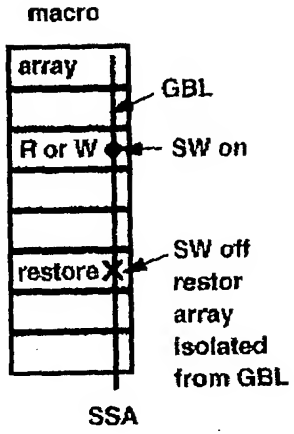

- Single cycle Read_restore converted into 2 cycles Read, restore pipeline
- restore cycle allows other banks to do concurrent Read/Write

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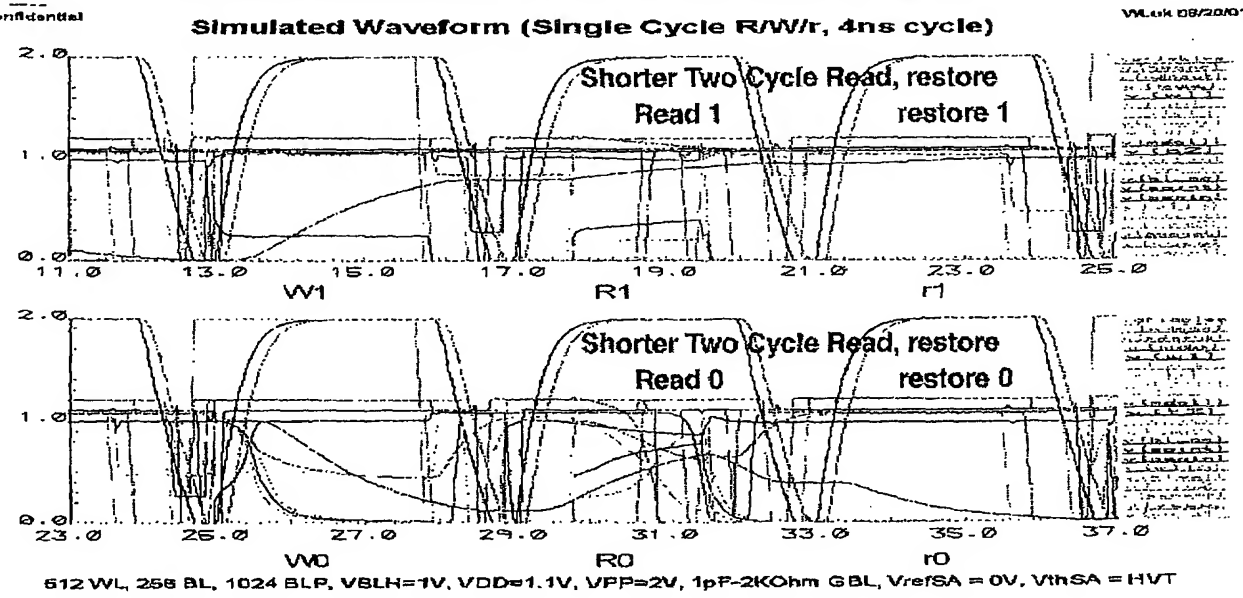

R/W/r pipeline allows:

Concurrent R, W and restor ops in different arrays in a macro

Fine grain controls for performance:

Destructive_Read (R)	1 cycle
Write (W)	2 cycle
Read_restore (Rr)	2 cycles
ReadModifyWrite(R,W)	2 cycles
Refresh (Rr)	2 cycles

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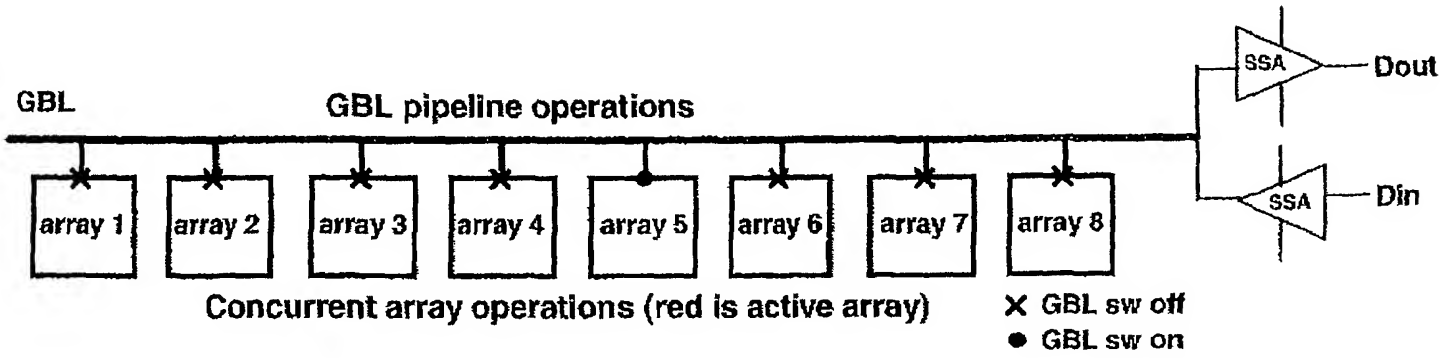
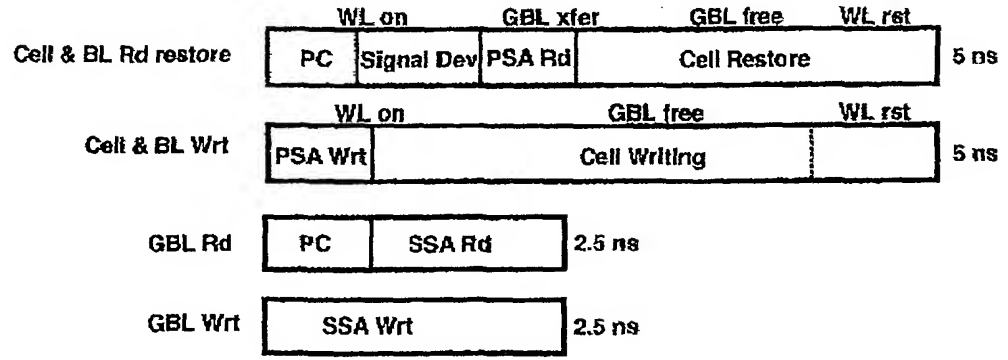
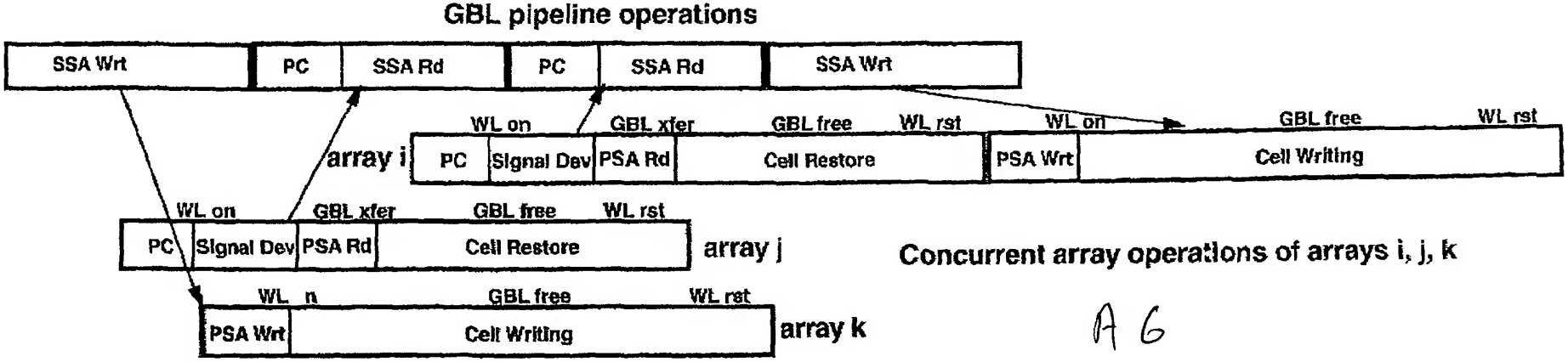
Concurrent Pipeline Operations of Arrays and GBL (potential)





Constraints:
T_cell ~ 2.5 - 3 ns
T_GBL ~ 1.5 ns (9Mb)

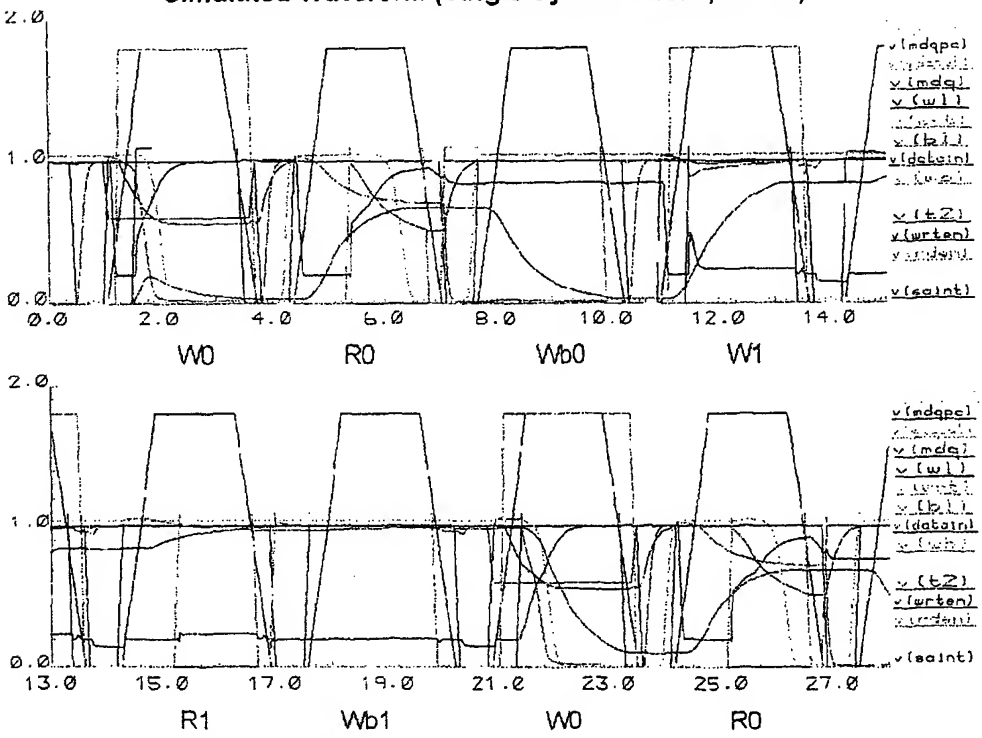
Possibilities
Trc = 5 ns
Trdd = 2.5 ns



Concurrent array operations of arrays i, j, k

A 6

Simulated Waveform (Single Cycle R/W/Wb, 3.3 ns)



256 WL, 128 BL, 1pF GBL, VrefSA = 0.2 V, VthSA = 0.3 V

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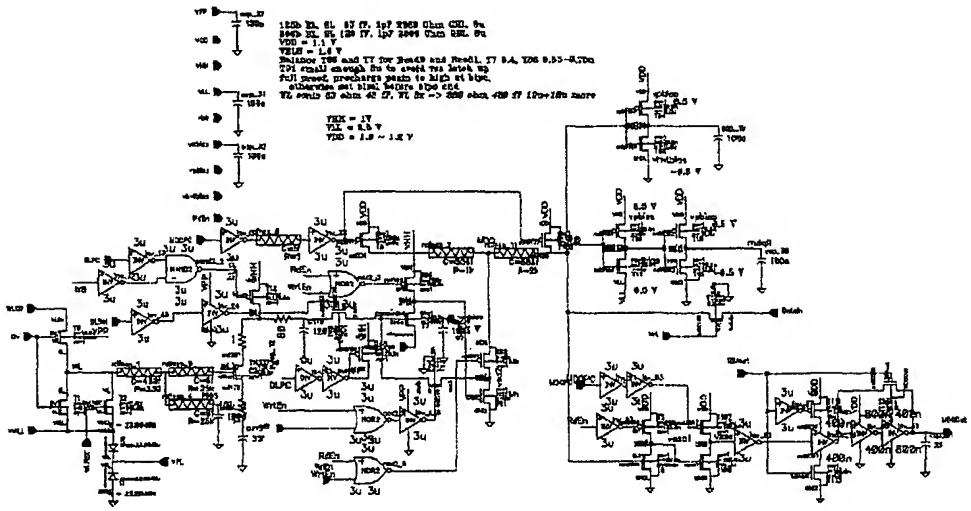
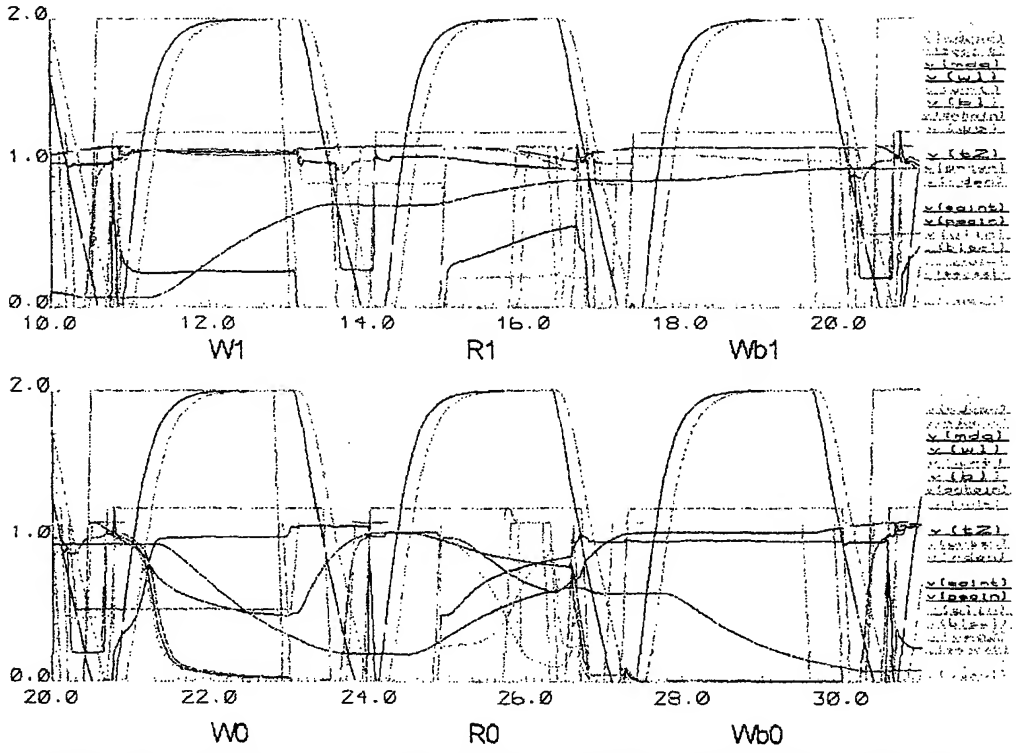
Circuit Simulation



512 WL, 256 BL, 1024 BLP, VBLH=1V, VDD=1.1V, VPP=2V, 1pF-2KOhm GBL

A 8

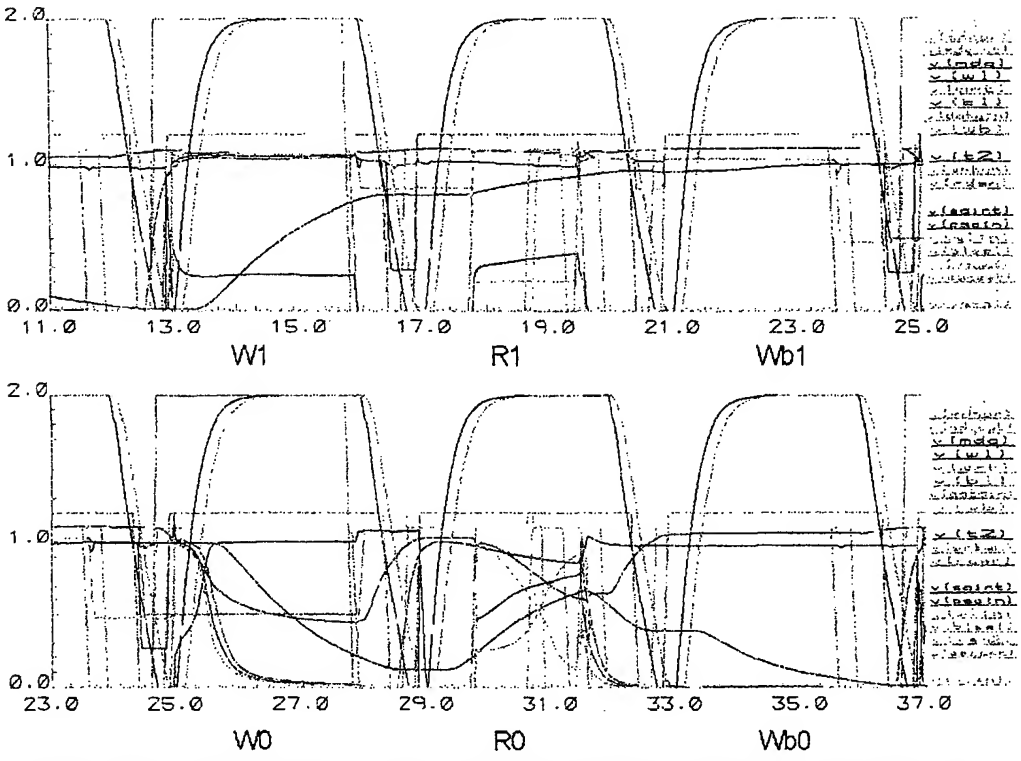
Simulated Waveform (Single Cycle R/W/Wb, 3.3 ns)



256 WL, 128 BL, 1024 BLP, VBLH=1V, VDD=1.1V, VPP=2V, 1pF-2KOhm GBL, VrefSA = 0V, VthSA = HVT

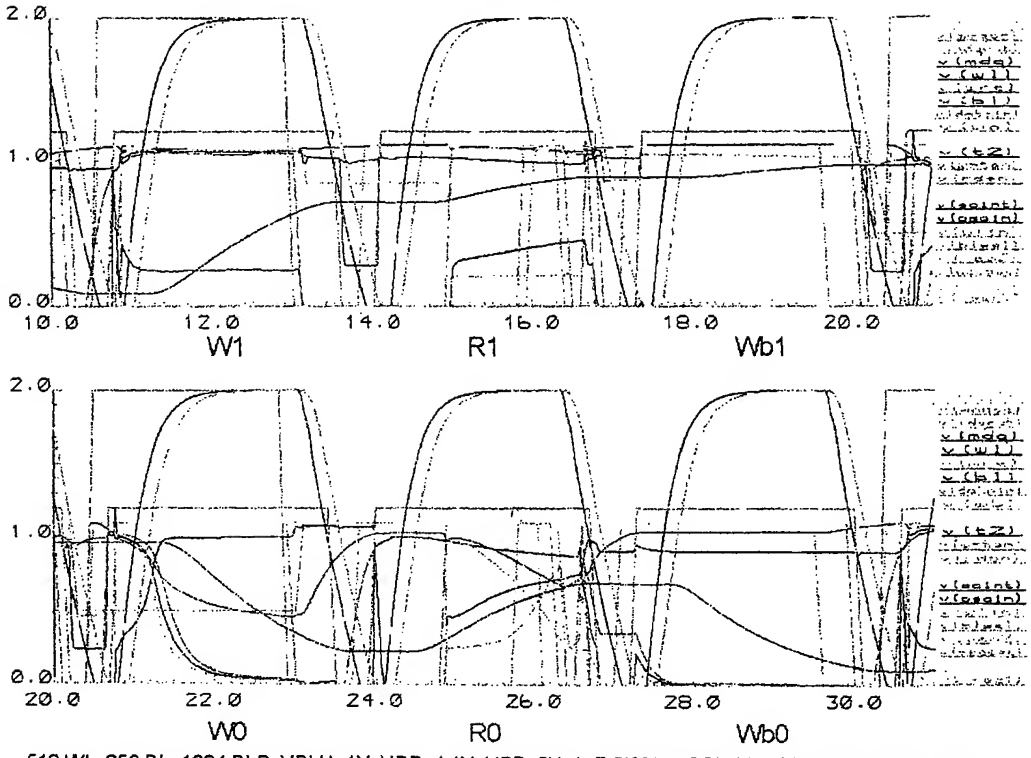
A 10

Simulated Waveform (Single Cycle R/W/Wb, 4ns cycle)



512 WL, 256 BL, 1024 BLP, VBLH=1V, VDD=1.1V, VPP=2V, 1pF-2KOhm GBL, VrefSA = 0V, VthSA = HVT

Simulated Waveform (Single Cycle R/W/Wb, 3.3 ns)



512 WL, 256 BL, 1024 BLP, VBLH=1V, VDD=1.1V, VPP=2V, 1pF-2KOhm GBL, VrefSA = 0V, VthSA = HVT

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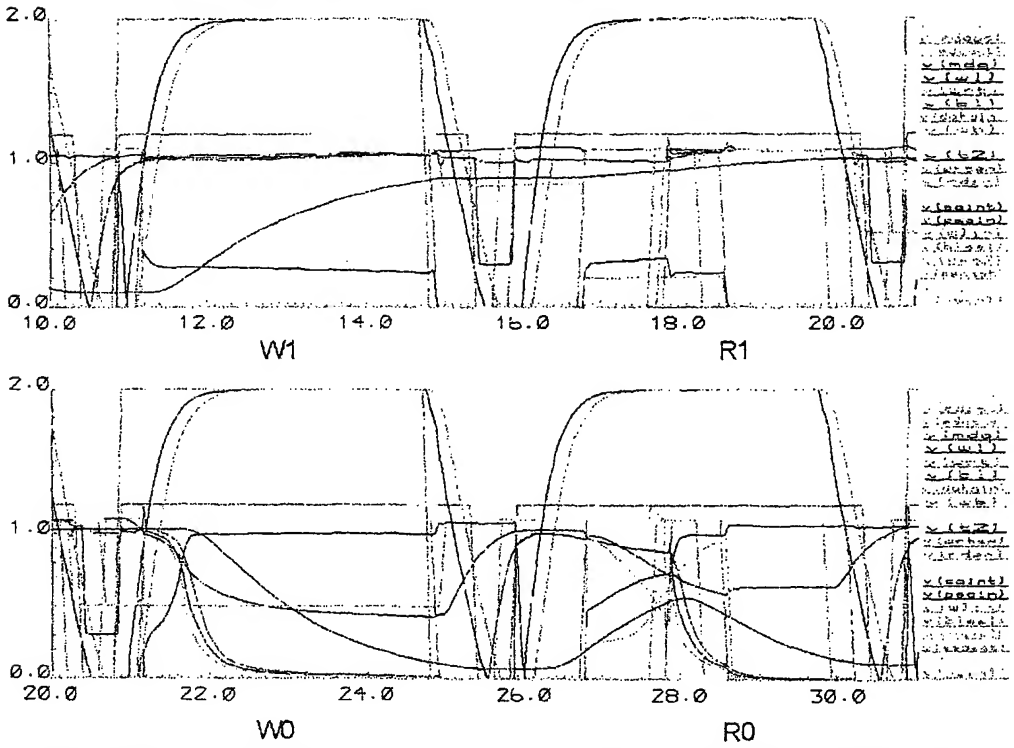
Simulated Waveform (Single Cycle W, RWb, 5 ns)



512 WL, 256 BL, 1024 BLP, VBLH=1V, VDD=1.1V, VPP=2V, 1pF-2KOhm GBL, VrefSA = 0V, VthSA = HVT

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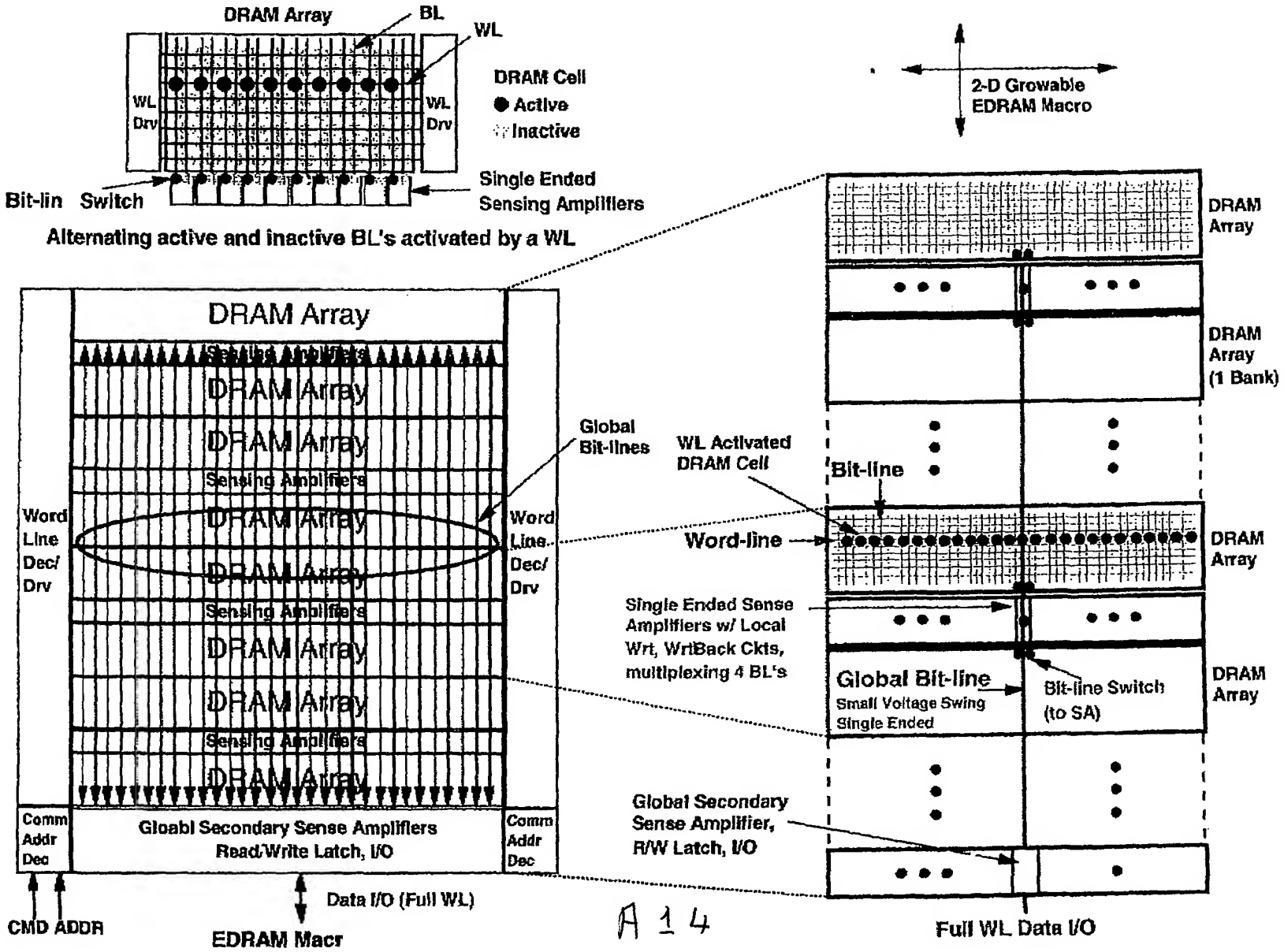
Low Power, Short Singl Cycle R/W/Wb Pipeline, Small Voltage Swing, Enhanced Write, Full-WL I/O, Multi-Bank EDRAM Macro



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